REMARKS

As requested, the specification has been reviewed. No errors in need of correction were noted.

The present amendment cancels claims 3, 7-18 and 21, and adds claim 25, leaving claims 1-2, 4-6, 19-20, and 22-24, which have been amended, and new claim 25 for consideration.

Claims 1-2, 4-6, 15, 19-20, and 22-24, were rejected as unpatentable over the Admitted Prior Art (APA) in view of SHIN et al. 5,974,464. Reconsideration and withdrawal of the rejection are respectfully requested.

Amended claims 1 and 19 provide, among other features, that the changing-point counter conducts its counting operation for (n + 1)-bit serial code by including a last bit of an immediately preceding n-bit serial code the encoder has dealt to the n-bit serial data. By contrast, the transition counter 74 in SHIN et al. (column 11, lines 30-53; column 12, lines 16-17) considers only the transitions within a byte; it does not include a last bit of an immediately preceding code as in amended claims 1 and 19. Accordingly, this feature is missing from the proposed combination and therefore would not be obvious to one of skill in the art.

The claims have also been amended to refer to a "first value" instead of "true" so as to include devices that use either true or false.

Consideration of new claim 25 is respectfully requested. This claim is directed to the fourth embodiment that is discussed beginning at page 55 and shown in Figure 11. While this embodiment was indicated to be a fourth species of the invention (which was not elected), the embodiment defined in claim 25 is sufficiently similar to the embodiment defined in the elected species so as to be considered with the elected species. For example, claim 25 includes the same limitations as claim 1, plus the delay circuit that defines a delayed discrimination bit.

New claim 25 is allowable for the reasons set forth above for claim 1 and for the further reason that the references do not disclose the delayed discrimination bit claimed in claim 25. By way of explanation (and with reference to Figure 11 and the discussion the fourth embodiment beginning at page 55), the output of the two-input OR gate 24 (i.e., the output of the changing-point counting circuit 2) is fed back to the delay circuit 25. The output of the two-input OR gate 24 is input to the parallel-to-serial conversion circuit 5 as the discrimination bit 8'. The output of the delay circuit 25 is input to the EXOR gate 21 located at the lowest position along with the LSB (bit 0) of the 8-bit data, thereby detecting whether these two bits have different values.

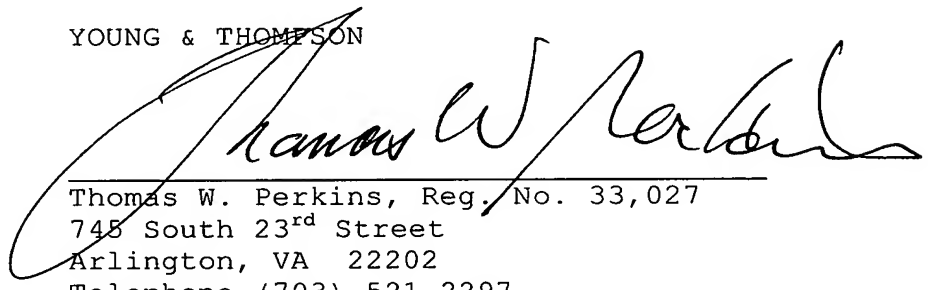
In view of the present amendment and the foregoing remarks, it is believed that the present application has been

placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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